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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/075,783	02/14/2002	Claude Gauthier	03226.163001;P7058	9162

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EXAMINER	
FERRIS III, FRED O	

ART UNIT	PAPER NUMBER
2128	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/075,783	GAUTHIER ET AL.	
	Examiner	Art Unit	
	Fred Ferris	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 February 2002*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 January 2006* is/are: a)☒ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. *Claims 1-33 have been presented for examination based on applicant's amendment filed 8 December 2005. Claims 1-33 remain rejected by the examiner.*

Response to Arguments

2. *Applicant's arguments filed 8 December 2005 have been fully considered but they are not persuasive.*

Regarding applicant's response to double patenting rejection: Applicants are reminded that the nonstatutory double patenting rejection is based on obviousness and are directed to MPEP 804. MPEP 804 recites the following:

> *"If the application at issue is the later filed application* ***or both are filed on the same day****, only a one-way determination of obviousness is needed in resolving the issue of double patenting, i.e., whether the invention defined in a claim in the application *>would have been< an obvious variation of the invention defined in a claim in the patent. See, e.g., In re Berg, >140 F.3d 1438,< 46 USPQ2d 1226 (Fed. Cir. 1998) (the court applied a one-way test where both applications were filed the same day). If a claimed invention in the application *>would have been< obvious over a claimed invention in the patent, there would be an unjustified timewise extension of the patent* ***and an obvious-type double patenting rejection is proper****."*

The examiner therefore maintains the nonstatutory obviousness-type double patenting rejection as recited below.

Regarding applicant's response to 103(a) rejection: The examiner first notes that the amendment to the claims has not clearly distinguished the claimed subject matter as non-obvious over the prior art. The main thrust of applicant's arguments center around arguing that the combination of prior art references does not teach or render obvious (a) estimating jitter of a delay locked loop depending on the an input representative power supply waveform, and (b) adjusting an amount of decoupling capacitance dependent on

the estimating. In response the examiner notes that, as indicated in applicants response (page 10, line 18), and in applicant's specification (para: 0020), the present invention is drawn to a technique for optimizing decoupling capacitance in a delay locked loop. Applicants have also disclosed that "jitter is related to power supply noise" (para: 0006). In fact, paragraph 0041 of the specification appears to indicate that a byproduct of reducing the power supply noise, is a direct reduction in circuit jitter. There does not appear to be anything disclosed in applicant's specification to indicate that the jitter is actually estimated by any other method than through a direct measurement of noise. Applicant's arguments that Zhu is directed to margins for noise, and not jitter are therefore not persuasive.

Paragraph 0021 of the specification then indicates that the jitter is estimated until the jitter falls below a selected amount (i.e. a threshold). Clearly, both the prior art and the present invention are concerned with optimizing the amount of capacitance applied to the circuit based on an established threshold. That is, the process of "estimating" as claimed in the present invention appears to simply involve a comparison to an established threshold. This feature is clearly disclosed by Zhu as noted below. Further, both Zhu and the present invention set forth that the amount of decoupling capacitance is modified (para:0030) based on the results of a comparison (test) to see if jitter (noise related) falls below a selected amount (i.e. a threshold). Webster's defines the term "estimating" as "to calculate the amount or extent of". In this case both Zhu and the present invention appear to perform "estimation" process, by a calculation that simply involves a comparison to a threshold (i.e. selected amount). It is also noted that Zhu is

clearly concerned with an estimation decoupling capacitance based on the amount of noise margin (CL4-L7-12) in the circuit as is the present invention (para:0021, 0030, 0041). Further, all of the prior art techniques disclosed in Figures 1-3 render obvious the limitations relating to a model "dependent on the inputting".

Applicant's arguments and that AAPA fails to disclose "each and every limitation of the claimed invention", and that Culler, fails to teach "estimating jitter dependent on a power supply input", appear to be piecemeal since the rejection is based on obviousness. In this case AAPA is only relied upon for a teaching of estimating the jitter of a delay locked loop, while Culler is relied upon only for a teaching of a simulated power supply inclusive of waveform temperature, voltage, and frequency parameters. One cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See In re Keller, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); In re Merck & Co., 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). The examiner therefore maintains the 103(a) rejection of claims 1-33 as noted below.

Regarding applicant's submission of formal drawings: The examiner has approved Applicant's formal drawings submitted 6 January 2006.

Preamble of the Claims

3. The preambles of independent claims 1, and 12 as presented for examination, have not been given patentable weight. Appropriate weight is given to limitations recited in the body of the claim that are needed for purpose of antecedence. "A mere

statement of purpose or intended use in the preamble of a claim need not be considered in finding anticipation; however, it must be considered if the language of a preamble is necessary to give meaning to the claim" Diversitech Corp. v. Century Steps, Inc., 7 USPQ2d 1315 (Fed. Cir. 1988); In re Stencel, 4 USPQ2d 1071 (Fed. Cir. 1987)

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

4. Claims 1 - 33 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1 - 33 of copending Application No. 10/075,757. Although the conflicting claims are not identical, they are not patentably distinct from each other because the method, apparatus, and computer medium claims of the present invention are nearly identical in verse to the method, apparatus, and computer medium claims of Application No. 10/075,757, with the exception of the recitation "delay locked loop" as opposed to the recitation of "phase

locked loop" in the 757' application. Further, both the present invention and Application No. 10/075,757 claim the same limitations (i.e. technique) for optimizing a decoupling capacitance, namely, inputting a power supply waveform, estimating the jitter, and adjusting the amount of decoupling capacitance until the jitter falls below a selected amount. Accordingly, it would have been obvious to a skilled artisan to apply decoupling capacitance techniques of inputting a power supply waveform, estimating the jitter, and adjusting the amount of decoupling capacitance until the jitter falls below a selected to a delay locked loop circuit, as opposed to the phase locked loop circuit, since the decoupling "optimization" process can obviously be applied by a designer to either type of circuit. (See Fig. 3, page 4, para: 0009, present invention, Fig. 4, 757' application)

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein

were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claims 1-6, 12-17, and 23-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,446,016 issued to Zhu in view of applicants admission that inputting a power supply waveform having noise and estimating jitter of a delay locked loop is known in the art.

Independent claims 1, 12, and 23 are drawn to:

Method, system, and computer medium for optimizing decoupling capacitance in a delay locked loop by:

a) inputting representative power supply waveform noise delay locked loop simulation;
b) estimating jitter of delay locked loop;
c) adjusting amount of decoupling capacitance;
d) repeating a-c until jitter falls below selected amount.

Regarding independent claims 1, 12 and 23: Zhu teaches a computer based method and system for optimizing the decoupling capacitance in a circuit design by adjusting the amount of decoupling capacitance (Abstract, CL7-L5-20, Figs. 3, 7) in accordance with predetermined (selected) specification values inclusive of repeating the adjusting process (CL7-L62-63) to find the optimal decoupling capacitance value relative to power supply noise. (Background, CL3-L1-37)

Zhu does not explicitly disclose inputting a power supply waveform having noise or estimating jitter of a delay locked loop.

Applicant's specification discloses that the claimed elements relating to inputting a power supply waveform having noise, and estimating jitter of a delay locked loop were known a prior art at the time of the invention. Specifically, in the specification, applicants disclose that the prior art approach shown in Figure 3 discloses the elements of inputting a representative power supply waveform (including noise) into a delay locked loop (specification page 7, para: 0024). In the background of the invention applicants further disclose the "common" performance measure of delay locked loop jitter (specification page 2, para: 6, Fig. 2). Both Figures 2 and 3 are designated as prior art. The examiner therefore submits that applicants have merely claimed features that have been disclosed as prior art, with subsequent optimization of the decoupling capacitance by adjusting the capacitance in accordance with predetermined specification values as disclosed by Zhu.

It would have been obvious to one having ordinary skill in the art at the time the claimed invention was made to modify the teachings of Zhu relating to optimizing the decoupling capacitance in a circuit design by adjusting the amount of decoupling capacitance, with the features relating to inputting a power supply waveform having noise, and estimating jitter of a delay locked loop as admitted by applicants, to realize the elements of the claimed invention. An obvious motivation exists, since Zhu discloses that circuit performance and noise budget are improved by decoupling capacitor optimization in a circuit. (See Zhu: Abstract) Accordingly, a skilled artisan

tasked with realizing a system and method optimizing the decoupling capacitance in a delay locked loop circuit, would have knowingly modified the teachings of Zhu with the prior art jitter estimation techniques as admitted by applicants, to realize the claimed elements of the present invention.

Per dependent claims 2-5, 13-16, and 24-27: Zhu teaches that the power supply, circuit board, chip package, and chip (IC) are comprised as part of the physical system (CL1-L10-47).

Per dependent claims 6, 17, and 28: Zhu teaches that it is desirable to locate the optimal decoupling near (adjacent) to the location of the source node. (CL5-L17- 47) In this case the DLL power supply. Hence, a skilled artisan would have knowingly represented the power supply waveform adjacent to an intended DLL location using the reasoning previously cited above.

6. Claims 7-11, 18-22, and 29-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,446,016 issued to Zhu in view of applicants admission (noted above) and in further view of U.S. Patent 6,370,678 issued to Culler.

Per dependent claims 7-11, 18-22, and 29-33: The combination of Zhu and admitted prior art by applicants as noted above renders obvious the limitations recited in independent claims 1, 12, and 23 as previously cited.

The combination of Zhu and admitted prior art by applicants does not explicitly disclose the elements of a simulated power supply including waveform, temperature, voltage, and frequency.

Culler teaches a simulated power supply (Abstract, Figs. 3-10) inclusive of waveform (CL1-L55-67, CL4-L45-67), temperature, voltage, and frequency parameters (CL3-L9-53, Figs. 6-10.

Hence a skilled artisan would have knowingly further modified the teachings of Zhu and the prior art admitted by applicants, with the teachings of Culler to realize the claimed limitations of claims 7-11, 18-22, and 29-33 using the same reasoning previously cited above.

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, ***THIS ACTION IS MADE FINAL****. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).*

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

"Analysis fo Jitter due to Power-Supply Noise in Phase-Locked Loops, Heydari, IEEE Custom Integrated Circuits Conference, IEEE 2000

U.S. Patent 6,782,347 issued to Hirano et al teaches optimizing decoupling capacitance in a printed circuit.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fred Ferris whose telephone number is 571-272-3778 and whose normal working hours are 8:30am to 5:00pm Monday to Friday. Any inquiry of a general nature relating to the status of this application should be directed to the group receptionist whose telephone number is 571-272-3700. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jean Homere can be reached at 571-272-3780. The Official Fax Number is: 571-273-8300

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